CS105 – Computer Systems Spring 2020

Problem Session 2: Virtual Memory

SOLUTION

Wednesday, April 8, 2020

1. Assume you are working on a system with 16-bit virtual addresses, 14-bit physical addresses, and 1024 byte pages.

   (a) Draw a diagram that depicts the bits of the virtual address and indicate (by labeling the diagram) the bits that would be correspond to the virual page number and to the virtual page offset.

6-bit VPN	10-bit offset

   (b) Draw a diagram that depicts the bits of the physical address and indicate (by labeling the diagram) the bits that would correspond to the physical frame number and the physical frame offset.

4-bit FN	10-bit offset

2. Assume that you are running on the system described in Problem 1 and the current page table state is as follows (note that all numbers are in hex):

Page Table					
VPN	PFN	Valid	VPN	PFN	Valid
00	NULL	0	10	0	1
01	5	1	11	E	1
02	7	1	12	9	0
03	9	0	13	7	1
04	F	1	14	D	1
05	3	1	15	5	0
06	B	0	16	E	1
07	D	1	17	6	0
08	7	1	18	1	0
09	C	0	19	E	1
0A	NULL	0	1A	8	1
0B	1	1	1B	NULL	0
0C	0	1	1C	NULL	0
0D	D	0	1D	2	1
0E	0	0	1E	7	0
0F	6	0	1F	3	0

   For the given virtual addresses, indicate the virtual page number (VPN) and offset (VPO). Then determine whether a page fault occurs (Y/N). If there is no page fault, specify the corresponding physical frame number (PFN) and physical address.

Virtual Address	VPN	VPO	Page Fault?	PFN	Physical Address
0x6A47	1A	247	No	8	2247
0x3442	0D	042	Yes		

3. Assume that this system also has a 4-way set associative TLB with 16 total entries. Modify your solution to Problem 1 to indicate which bits correspond to the TLB tag and which bits correspond to the TLB index.

   The last two bits of the page number of the TLBI. The high-order four bits of the page number are the TLBT.

4. Assume that the contents of the TLB are as shown below, and the first 32 pages of the page table are depicted in Problem 2.

TLB												
Index	Tag	PFN	Valid	Tag	PFN	Valid	Tag	PFN	Valid	Tag	PFN	Valid
0	8	7	1	F	6	1	0	3	0	1	5	1
1	1	1	1	2	7	0	7	3	0	4	E	1
2	0	0	0	C	1	0	F	8	1	7	6	1
3	8	4	0	3	5	0	0	D	1	2	9	0

   For the given virtual addresses, indicate the virtual page number (VPN), TLB index (TLBI), and TLB tag (TLBT). Then indicate whether the TLB hits (Y/N) and whether there is a page fault. If there is a page fault, leave the physical address blank. Assume that all numbers are given in hex.

Virtual Address	VPN	TLBI	TLBT	TLB Hit?	Page Fault?	PFN	Physical Address
0x2F09	0B	3	2	N	N	1	0709
0x4747	11	1	4	Y	N	E	3B47

5. Suppose a machine with 32-bit virtual addresses and 40-bit physical addresses is designed with a two-level page table, subdividing the virtual address into three pieces as follows:

10 bit idx1	10 bit idx2	12 bit offset

   The first 10 bits are the index into the page directory, the second 10 bits are the index into the second-level page table, and the last 12 bits are the offset into the page. There are 3 protection bits and valid bit per page, so each page table entry takes 4 bytes.

(a) What is the page size in this system?

4096 bytes (4KB)

(b) How much memory is consumed by the first and second level page tables for a process that has 100KB of memory starting at address 4048?

100KB is 25 pages, so the second level page table will need to contain 25 page table entries. Each of these will take 4 bytes, so the second-level page table will need 100 bytes of memory. This means the second-level page table will fit comfortably in one page of memory, so there will only be one page directory entry in the first level page table (taking up 4 bytes). So the total memory consumed by the first and second level page tables would be 105 bytes.